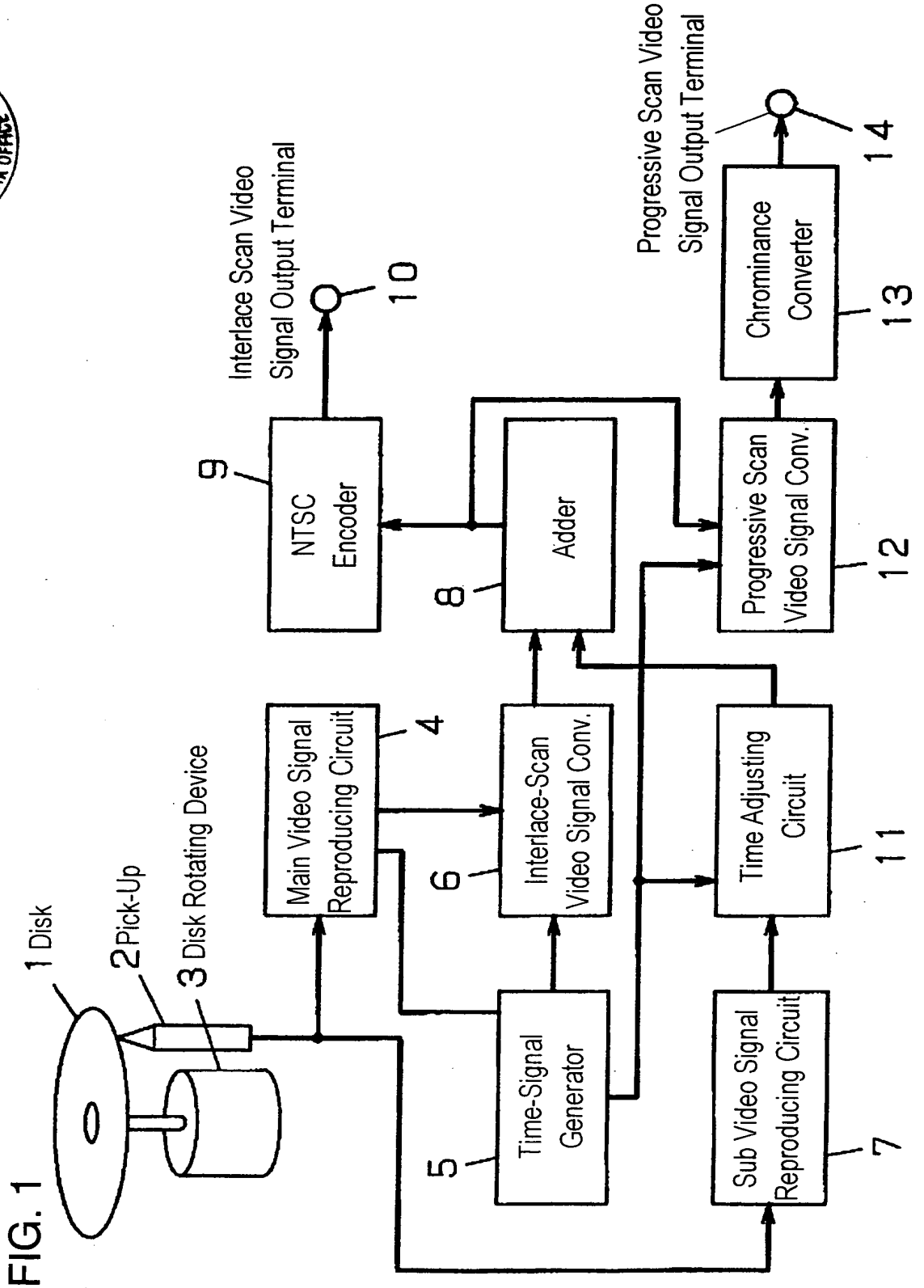


FIG. 1

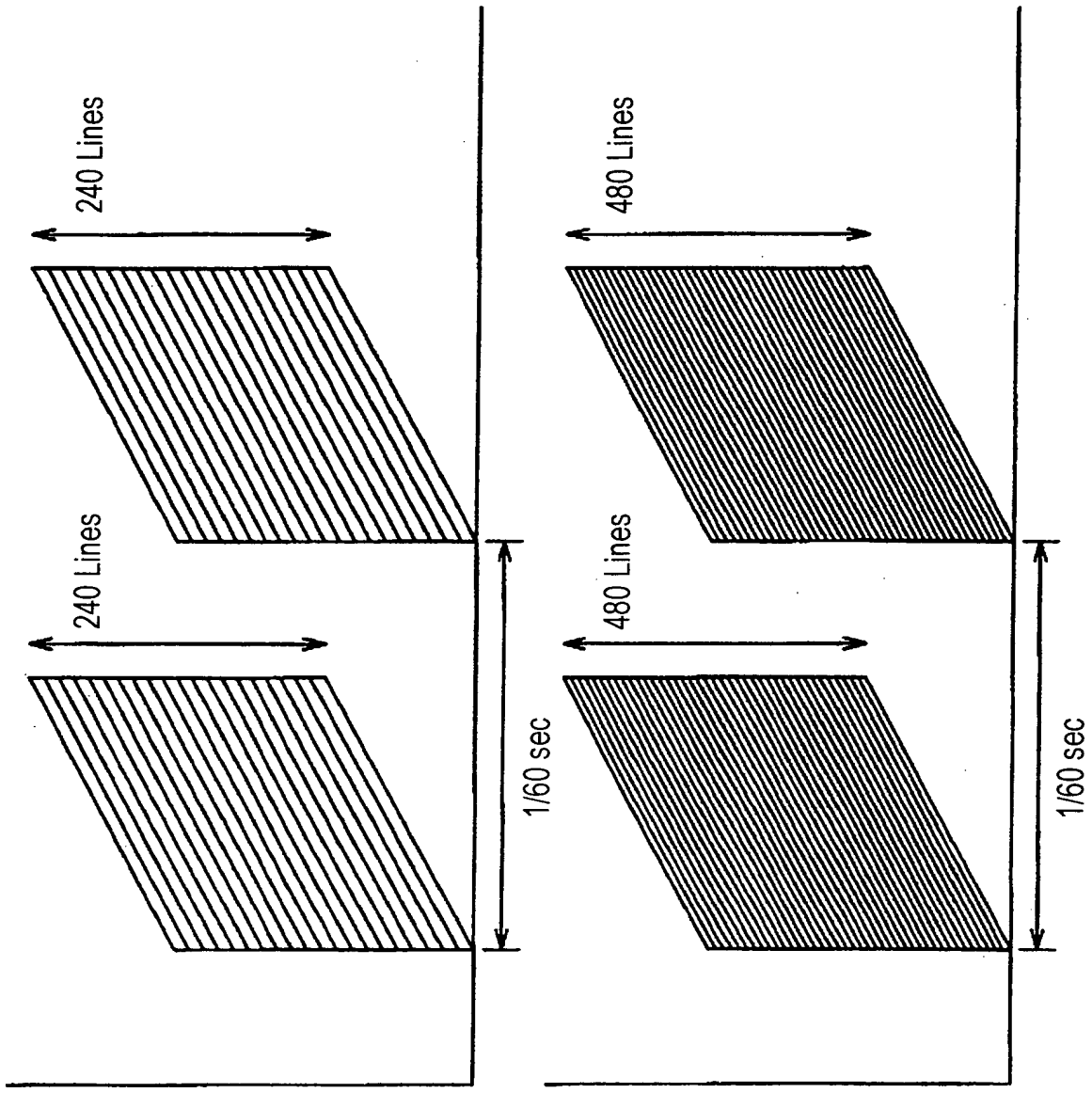
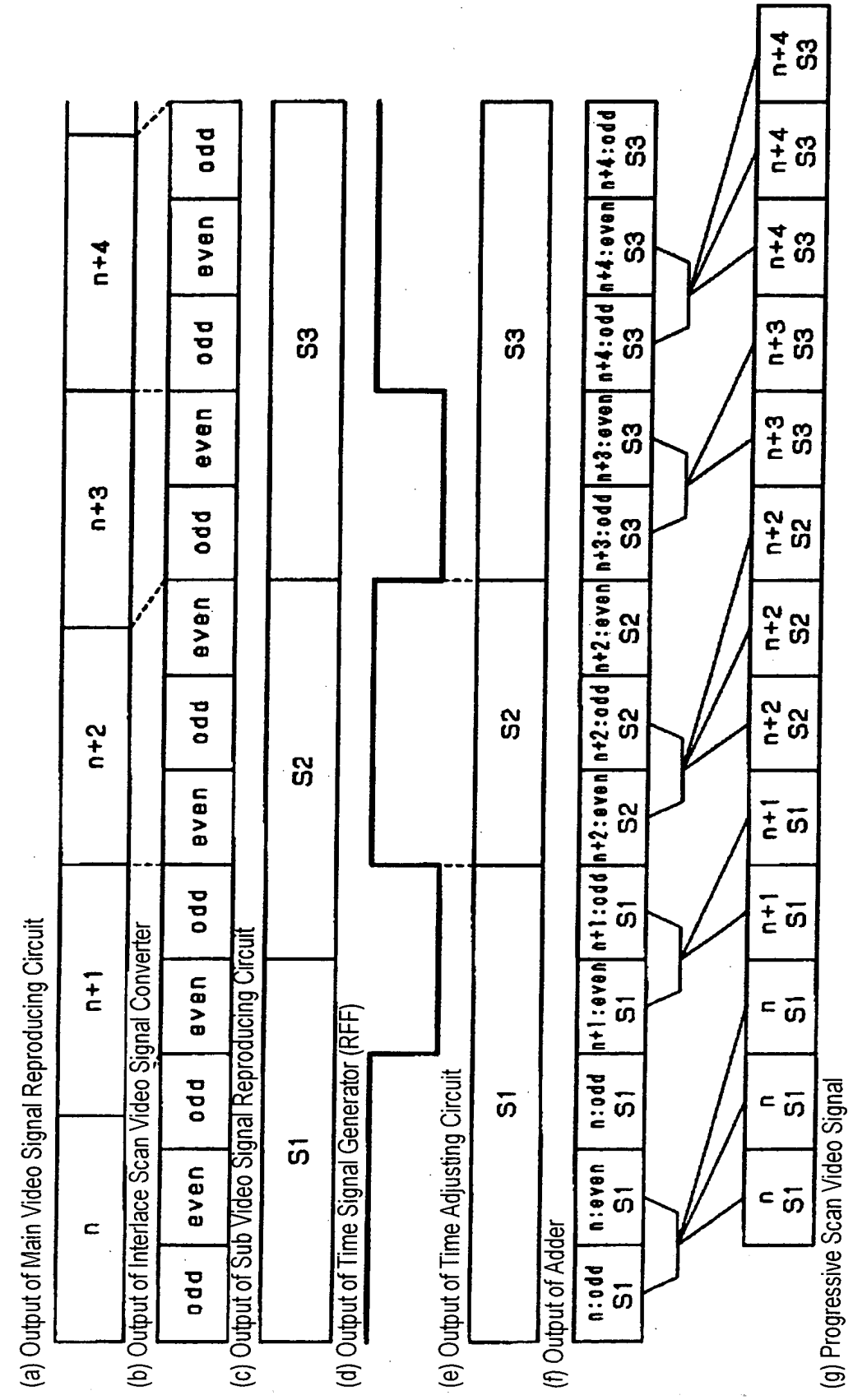


FIG. 2

FIG. 3


(a) Output of Main Video Signal Reproducing Circuit
n
n+1
n+2
n+3
n+4
(b) Output of Interlace Scan Video Signal Converter
odd
even
odd
even
odd
even
odd
even
odd
(c) Output of Sub Video Signal Reproducing Circuit
S1
S2
S3
(d) Output of Time Signal Generator (RFF)
(e) Output of Time Adjusting Circuit
(f) Output of Adder
n:odd S1
n:even S1
n:odd S1
n+1:even S1
n+1:odd S1
n+2:even S2
n+2:odd S2
n+2:even S2
n+3:odd S3
n+3:even S3
n+4:odd S3
n+4:even S3
n+4:odd S3
(g) Progressive Scan Video Signal
n S1
n S1
n+1 S1
n+1 S1
n+2 S2
n+2 S2
n+3 S3
n+3 S3
n+4 S3
n+4 S3
n+4 S3

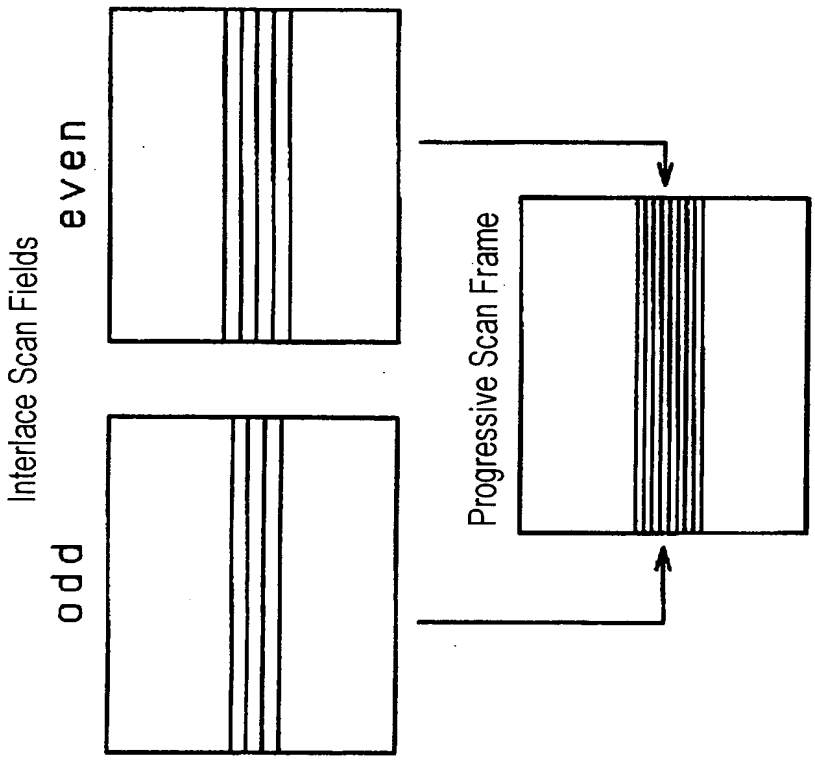


FIG. 4

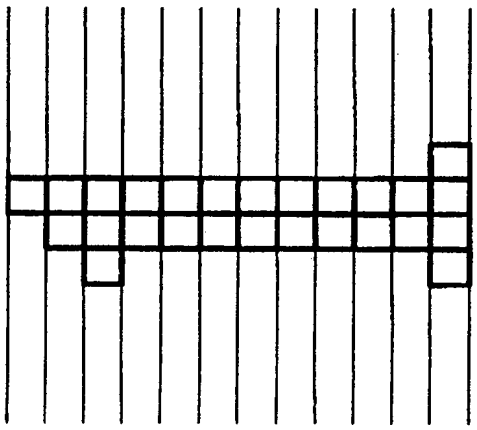


FIG. 5

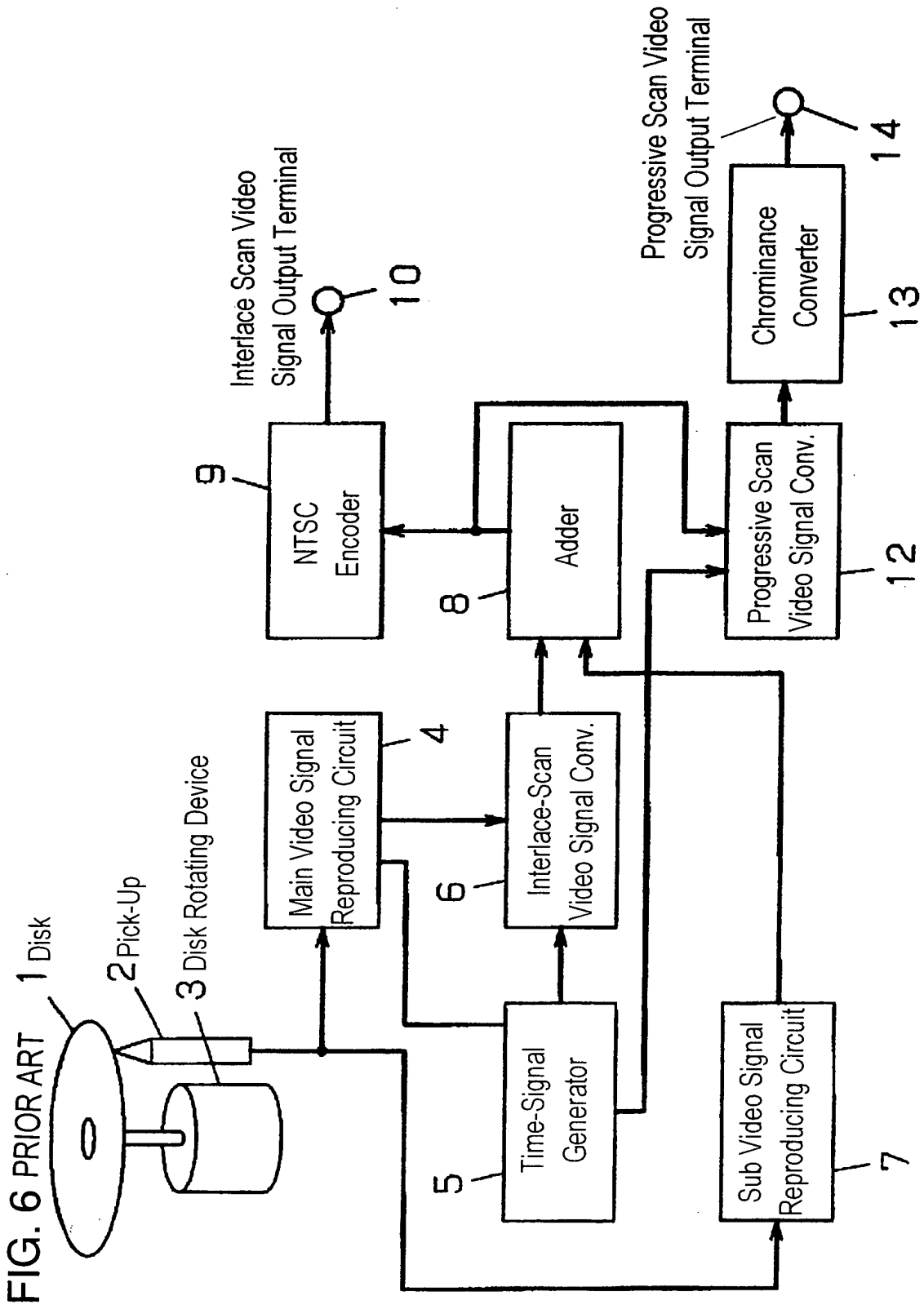


FIG. 6 PRIOR ART

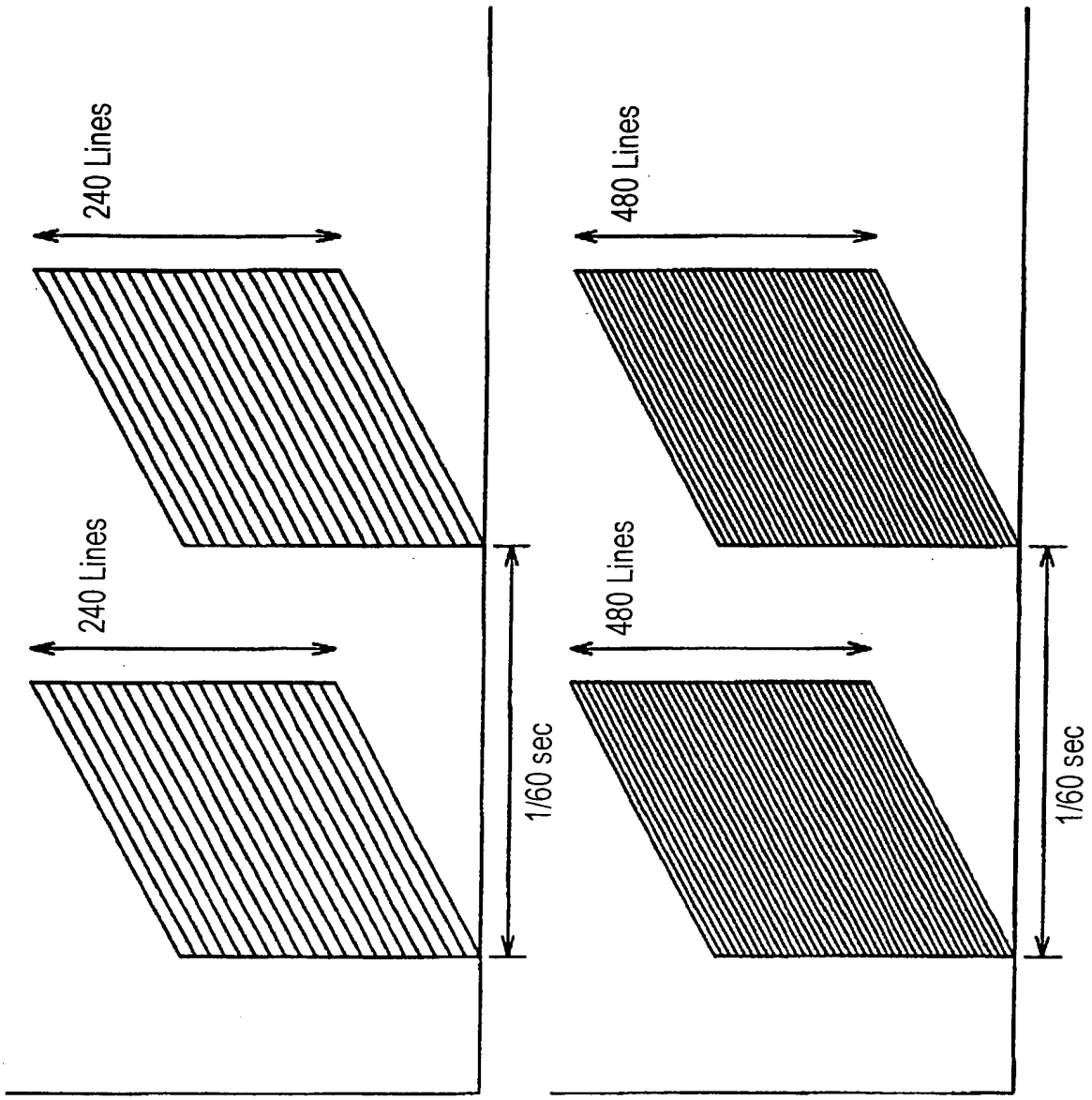
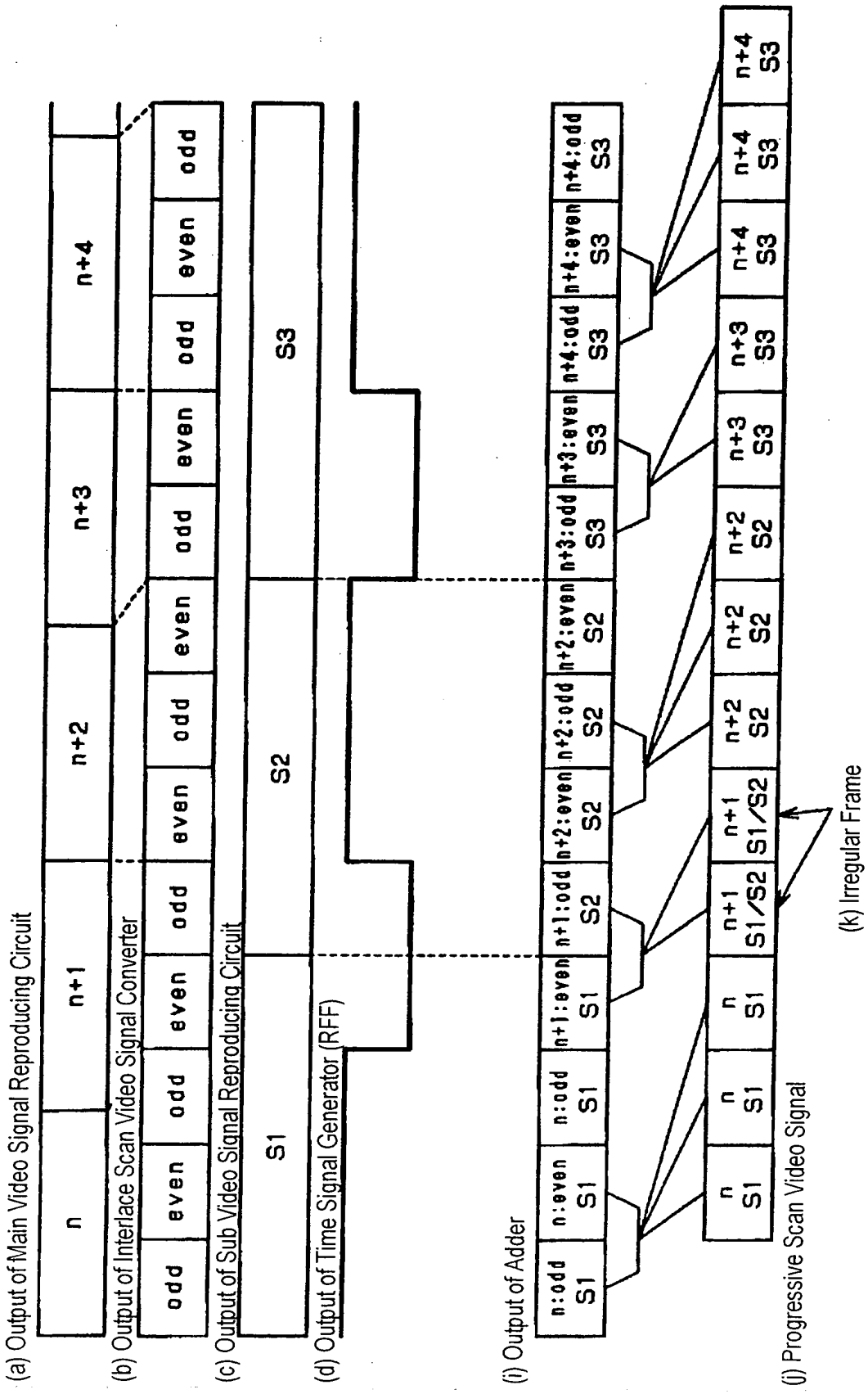


FIG. 7
PRIOR ART

FIG. 8 PRIOR ART



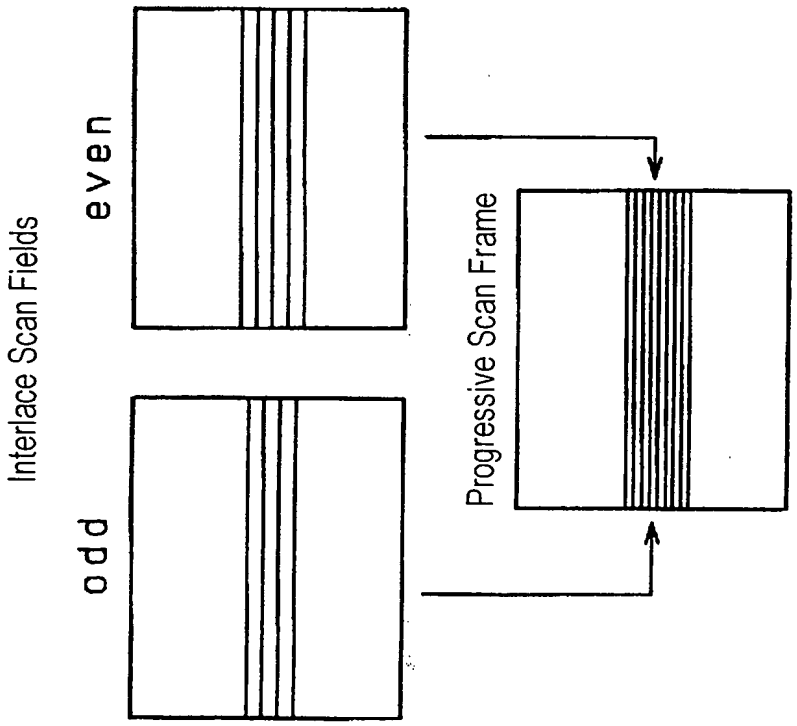


FIG. 9
PRIOR ART

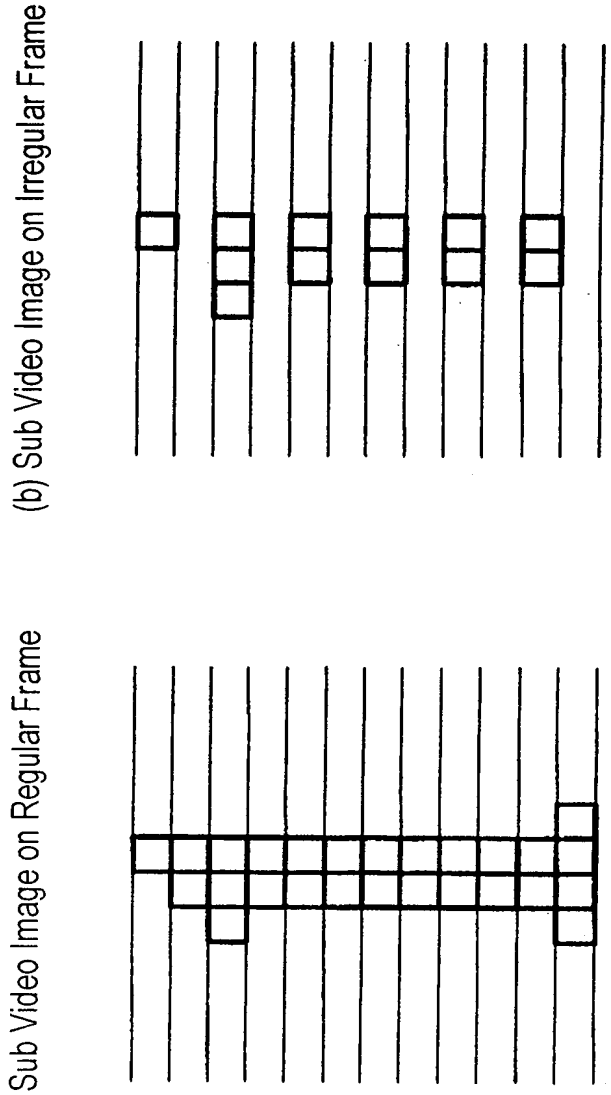


FIG. 10
PRIOR ART